AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the captioned patent application:

Listing of Claims:

1. (Currently Amended) In an electronic system, a system for voltage margin testing of one or more components of said system, comprising:

a Baseboard Management Controller (BMC) that implements ~~an Intelligent Platform Management Interface (IPMI)~~ a protocol, wherein the BMC[[-]] is internal to said electronic system; ~~and~~

a digital voltage adjuster configured to communicate with said BMC~~controller~~ and to affect generation of one or more test voltages for application to said one or more components in response to commands from the BMC~~controller~~; and

an Inter-Integrated Circuit (I^2C) based bus for providing communication between said BMC and said digital voltage adjuster.

2. (Previously Presented) The margin testing system of claim 1, further comprising:

diagnostics software capable of collecting and analyzing data regarding a response of said system to said test voltages.

3. (Currently Amended) The margin testing system of claim 1, further comprising:

a power rail electrically coupled to said components for applying voltage thereto, said digital voltage adjuster being electrically coupled to said power rail to set said power rail voltage to one or more of said test voltages.

4. (Currently Amended) The margin testing system of claim 3, further comprising:

a voltage regulator configured to receive an input voltage and generate a regulated output voltage for application to said power rail, said digital voltage adjuster being coupled to said voltage regulator for varying said regulated output voltage in response to commands from said BMC controller.

5. (Currently Amended) The margin testing system of claim 4, wherein said digital voltage adjuster comprises:

a digital potentiometer incorporated in a feedback circuitry of said voltage regulator,

wherein the digital potentiometer is configured to vary a resistance associated with said feedback circuitry in response to commands from said BMC ~~controller~~ so as to vary said output voltage of the voltage regulator.

6. (Currently Amended) The margin testing system of claim 4, further comprising:

a hardware monitor in communication with said voltage regulator and said BMC~~controller~~, said hardware monitor configured to measure said output voltage of said voltage regulator and transmit said measured voltage to said BMC~~controller~~.

7. (Currently Amended) The margin testing system of claim 6, wherein said BMC~~controller~~ is further configured to query said hardware monitor periodically to receive said measured voltage and wherein, said BMC~~controller~~ is further configured to transmit a feedback command to said digital voltage adjuster based on said measured voltage to cause the digital voltage adjuster to vary the output voltage of the voltage regulator from said measured value to a selected test value.

8-10. (Canceled)

11. (Currently Amended) The margin testing system of claim 1, wherein said BMC ~~controller~~ is configured to initiate margin testing in response to a command from an external system.

12. (Original) The margin testing system of claim 1, wherein said electronic system comprises:

a computer system.

13. (Original) The margin testing system of claim 12, wherein said computer system is a server.

14. (Currently Amended) A computer system, comprising:

a processor;

a plurality of components in communication with said processor for performing a plurality of tasks;

a Baseboard Management Controller (BMC) that implements ~~an Intelligent Platform Management Interface (IPMI)~~ a protocol; ~~and~~

a digital voltage adjuster configured to communicate with said BMC~~controller~~ affect generation of one or more test voltages for application to selected ones of said components for voltage margin testing thereof in response to commands from said BMC~~controller~~; and

an Inter-Integrated (I^2C) based bus for providing communication between said BMC and said digital voltage adjuster.

15-16. (Canceled)

17. (Previously Presented) The computer system of claim 14, further comprising:

a voltage regulator configured to receive an input voltage and generate a regulated output voltage for application to said components.

18. (Currently Amended) The computer system of claim 17, wherein said digital voltage adjuster comprises:

a digital potentiometer incorporated in a feedback circuitry of said voltage regulator said digital potentiometer configured to vary a resistance of said feedback circuitry in response to commands from said BMC~~controller~~ in order to set the output voltage of said voltage regulator to one or more of said test voltages.

19. (Currently Amended) A method for voltage margin testing of one or more components of an electronic system, having an internal Baseboard Management Controller (BMC) that implements ~~an Intelligent Platform Management Interface (IPMI)~~ a protocol and a digital voltage adjuster, the digital voltage adjuster in communication with said BMC and with at least a power rail supplying voltage to said components, comprising:

employing an Inter-Integrated Circuit (I^2C) based bus for providing communication between said BMC and said digital voltage adjuster

~~the BMC~~ transmitting one or more commands between the BMC [[to]] and said digital voltage adjuster to cause the digital voltage adjuster to affect generation of one or more test voltages at said power rail;

monitoring said electronic system to determine a response to each of said test voltages; and

storing information regarding a response of said electronic system to at least one of said test voltages.

20-21. (Canceled).

22. (Currently Amended) The method of claim 19, wherein monitoring said electronic system to determine a response comprising:

a hardware monitor measuring a voltage at said power rail and transmitting said measured voltage to said BMC~~controller~~.

23. (Currently Amended) In an electronic system, a system for voltage margin testing of one or more components of said system, comprising:

a Baseboard Management Controller (BMC) ~~controller~~ internal to said electronic system; and

a digital voltage adjuster configured to communicate with said BMC~~controller~~ and to affect generation of one or more test voltages for application to said one or more components in response to commands from the BMC~~controller;~~ ~~and~~

an Inter-Integrated (I^2C) based bus for providing communication between said BMC and said digital voltage adjuster;

a voltage regulator configured to receive an input voltage and generate a regulated output voltage for application to a power rail, said digital voltage adjuster being coupled to said voltage regulator for varying said regulated output voltage in response to commands from said BMC~~controller~~; and

a hardware monitor in communication with said voltage regulator and said BMC~~controller~~, said hardware monitor configured to measure said output voltage of said voltage regulator to determine a measurement value and transmit said measurement value to said BMC~~controller~~.

24. (Currently Amended) The margin testing system of claim 23, wherein said BMC~~controller~~ is further configured to query said hardware monitor periodically to receive said measurement value and wherein, said BMC~~controller~~ is further configured to transmit a feedback command to said digital voltage adjuster based on said measurement value to cause the digital voltage adjuster to vary the output voltage of the voltage regulator from said measurement value to a selected test value.

25. (Canceled).

26. (Previously Presented) The margin testing system of claim 23, wherein said BMC implements Intelligent Platform Management Interface (IPMI) Protocol.

27. (Canceled).

28. (New) The system of claim 1, wherein said protocol the BMC implements is an Intelligent Platform Management Interface (IPMI) Protocol.

29. (New) The computer system of claim 14, wherein said protocol that the BMC implements is an Intelligent Platform Management Interface (IPMI) Protocol.

30. (New) The computer system of claim 19, wherein said protocol that the BMC implements is an Intelligent Platform Management Interface (IPMI) Protocol.